CLAIMS

We claim:

1. A method for using memory, comprising the steps of:

performing read operations for a set of non-volatile storage elements associated with a first word line, said set of non-volatile storage elements are part of a group of non-volatile storage elements; and

prohibiting read operations for non-volatile storage elements in said group that are associated with other word lines.

2. A method according to claim 1, wherein:

said step of performing read operations includes applying a read compare voltage to said first word line and another voltage to said other word lines.

3. A method according to claim 1, wherein:

said group of non-volatile storage elements is a block of non-volatile storage elements.

4. A method according to claim 1, wherein:

said group of non-volatile storage elements are flash memory cells.

5. A method according to claim 1, wherein:

said group of non-volatile storage elements are NAND flash memory cells.

6. A method according to claim 1, wherein:

said group of non-volatile storage elements are NAND flash memory cells

arranged on a set of NAND strings;

said first word line connects to each of said NAND strings;

said other word lines connect to each of said NAND strings; and

said step of performing read operations includes applying a read compare voltage to said first word line and a pass voltage to said other word lines.

7. A method according to claim 1, wherein:

said group of non-volatile storage elements are multi-level NAND flash memory cells.

8. A method according to claim 1, wherein:

said group of non-volatile storage elements is a block of multi-level NAND flash memory cells;

said first word line is associated with a first logical page and a second logical page; and

said other word lines are associated with other logical pages.

9. A method according to claim 1, further comprising the steps of:

performing program operations for said non-volatile storage elements associated with said first word line; and

prohibiting program operations for said non-volatile storage elements in said group that are associated with said other word lines.

10. A method according to claim 9, wherein:

said group of non-volatile storage elements is a block of NAND flash memory cells arranged on a set of NAND strings;

said first word line connects to each of said NAND strings;

said other word lines connect to each of said NAND strings; and

said step of performing read operations includes applying a read compare voltage to said first word line and a pass voltage to said other word lines.

11. A method according to claim 9, wherein:

said non-volatile storage elements are multi-level NAND flash memory cells;

said first word line is associated with a first logical page and a second logical page; and

said other word lines are associated with other logical pages.

12. A method according to claim 1, wherein said steps of performing read operations and prohibiting read operations includes:

receiving a physical address for a particular read operation;

determining whether said physical address is valid;

performing said particular read operations if said physical address is valid; and

not performing said particular read operations if said physical address is not valid.

13. A method according to claim 1, wherein said steps of performing read operations and prohibiting read operations includes:

receiving a logical address for a particular read operation; and

mapping said logical address to a valid physical memory location associated with said first word line.

14. A method for using memory having a set of word lines, comprising the steps of:

performing read operations to one or more logical pages associated with a first control line of a block of non-volatile storage elements; and

prohibiting read operations to logical pages associated with other control lines of said block of non-volatile storage elements.

15. A method according to claim 14, wherein:

said non-volatile storage elements are NAND flash memory cells arranged on a set of NAND strings;

said first control line is a first word line that connects to each of said NAND strings;

said other control lines are other word lines that connect to each of said NAND strings; and

said step of performing read operations includes applying a read compare voltage to said first word line and a pass voltage to said other word lines.

16. A method according to claim 14, wherein:

said non-volatile storage elements are multi-level NAND flash memory cells.

17. A method for using memory, comprising the steps of:

performing read operations for a group of non-volatile storage elements associated with a particular word line; and

prohibiting read operations for non-volatile storage elements associated with one or more word lines that neighbor said particular word line.

18. A method according to claim 17, further comprising the steps of:

performing program operations for said group of non-volatile storage elements associated with said particular word line; and

prohibiting program operations for said non-volatile storage elements associated with word lines that neighbor said particular word line.

19. A method according to claim 17, wherein:

said group of non-volatile storage elements are NAND flash memory cells arranged on a set of NAND strings;

said particular word line connects to each of said NAND strings; and

said word lines that neighbor said particular word line connect to each of said NAND strings.

20. A method according to claim 17, wherein:

said group of non-volatile storage elements are multi-level NAND flash memory cells.

21. A method according to claim 17, wherein:

said group of non-volatile storage elements associated with said particular word line and said non-volatile storage elements associated with word lines that neighbor said particular word line are grouped together as a subset of a larger set of non-volatile storage elements

22. A method for using memory, comprising the steps of:

performing read operations to a first word line of a group of non-volatile storage elements; and

prohibiting read operations to all other word lines of said group of non-volatile storage elements.

23. A method according to claim 22, wherein:

said group of non-volatile storage elements is a block of NAND flash memory cells.

24. One or more processor readable storage devices having processor readable code embodied on said processor readable storage devices, said processor readable code for programming one or more processors to access non-volatile memory, said processor readable code:

allows read operations to one word line of a block of non-volatile storage elements; and

prohibits read operations to all other word lines of said block of non-volatile storage elements.

25. One or more processor readable storage devices according to claim 24, wherein said processor readable code:

allows program operations to said one word line; and

prohibits program operations to all other word lines of said block of non-volatile storage elements.

26. One or more processor readable storage devices according to claim 24, wherein:

said non-volatile storage elements are NAND flash memory cells arranged on a set of NAND strings;

said first word line connects to each of said NAND strings;

said other word lines connect to each of said NAND strings; and

said processor readable code programs said one or more processors to perform read operations that include applying a read compare voltage to said first word line and a pass voltage to said other word lines.

27. One or more processor readable storage devices according to claim 26,

wherein:

said non-volatile storage elements are multi-level NAND flash memory cells;

said first word line is associated with a first logical page and a second logical page; and

said other word lines are associated with other logical pages.

28. A memory system, comprising:

an array of non-volatile storage elements grouped into sets of non-volatile storage elements, each set of non-volatile storage elements being at least partially controlled by a set of word lines; and

a control system, said control system performs read operations for a first word line of a first set of said non-volatile storage elements and will not perform read operations for other word lines of said first set of said non-volatile storage elements.

29. A memory system according to claim 28, wherein:

said sets of non-volatile storage elements are blocks of non-volatile storage elements.

30. A memory system according to claim 28, wherein said control system:

determines whether a physical address is valid;

performs said read operations for said first word line if said physical address is valid; and

does not perform read operations for other word lines if said physical address is not valid.

31. A memory system according to claim 28, wherein:

said control system accesses a logical address for a particular read operation and

maps said logical address to a valid physical address associated with said first word line.

32. A memory system according to claim 28, wherein:

said first set of non-volatile storage elements are NAND flash memory cells arranged on a set of NAND strings;

said first word line connects to each of said NAND strings;

said other word lines connect to each of said NAND strings; and

said controller performs read operations for said first word line by applying a read compare voltage to said first word line and a pass voltage to said other word lines.

33. A memory system according to claim 28, wherein:

said non-volatile storage elements are multi-level NAND flash memory cells;

said first word line is associated with a first logical page and a second logical page; and

said other word lines are associated with other logical pages.

34. A memory system according to claim 28, wherein:

said control system performs program operations for said first word line of said first set of non-volatile storage elements and will not perform program operations for said other word lines of said first set of non-volatile storage elements.

35. A method for using memory, said memory including blocks of non-volatile storage elements, comprising the steps of:

identifying a block to be protected;

identifying a word line to be used in said block to be protected;

performing read operations to said word line to be used in said block to be protected; and

prohibiting read operations to all other word lines of said block to be protected.

36. A method according to claim 35, wherein said steps of performing and prohibiting includes:

determining if a physical address associated with a particular read operation is on said word line to be used in said block to be protected;

performing said particular read operation if said physical address is on said word line to be used in said block to be protected; and

not performing said particular read operation if said physical address is on a different word line in said block to be protected.

37. A method according to claim 35, wherein said steps of performing and prohibiting includes:

mapping a logical address to an appropriate physical location associated with said word line to be used in said block to be protected.

38. A method according to claim 35, further comprising the steps of:

performing program operations to said word line to be used in said block to be protected; and

prohibiting program operations to all other word lines of said block to be protected.

39. A method according to claim 35, wherein:

said non-volatile storage elements are NAND flash memory cells arranged on a set of NAND strings;

said word line to be used connects to each of said NAND strings; and

said other word lines connect to each of said NAND strings.

40. A method according to claim 35, wherein:

said non-volatile storage elements are multi-level NAND flash memory cells;

said word line to be used in said block to be protected is associated with a first logical page and a second logical page; and

said other word lines are associated with other logical pages.

41. A method according to claim 35, wherein:

said non-volatile storage elements are NAND flash memory cells.